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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,059	03/24/2004	Leonard Forbes	400.285US01	4221
27073	7590	12/13/2005		EXAMINER
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			ART UNIT	PAPER NUMBER
				2814

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/808,059	FORBES, LEONARD
	Examiner Marcos D. Pizarro-Crespo	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 11 October 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,2 and 4-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,2 and 4-7 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

Attorney's Docket Number: 400.285US01

Filing Date: 3/24/2004

Claimed Foreign Priority Date: none

Applicant(s): Forbes

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 10/11/2005.

Acknowledgment

1. The amendment filed on 10/11/2005 responding to the Office action mailed on 8/9/2005 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1, 2 and 4-7.

Claims Rejection

2. Initially, and with respect to claims 1, 2, and 4-7, note that a "product by process" claim is directed to the product *per se*, no matter how actually made. See *In re Thorpe*, 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in *Thorpe*, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re*

Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Note that the applicants have the burden of proof in such cases, as the above case law makes clear.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2, and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over She in view of Ahn (US 6514828).

5. Regarding claim 1, She shows (see, e.g., fig. 1) all aspects of the instant invention including an NROM memory transistor comprising:

- ✓ A substrate
- ✓ A plurality of source/drain regions in the substrate
- ✓ A nanolaminate, high permittivity (high-k), metal-gate dielectric having a dielectric constant greater than that of silicon dioxide (see, e.g., pp.53/col.1/ll.39-42)
- ✓ A control gate on top of the gate dielectric

wherein the conductivity type of the source/drain regions is different than that of the remainder of the substrate.

6. Regarding claim 2, She shows the gate dielectric is a composite oxide -- high-k dielectric – oxide nanolaminate gate insulator wherein the high-k dielectric is a charge-trapping layer (see, e.g., pp.53/col.1/II.1-7).

7. Regarding claim 5, She shows the charge-trapping layer comprising a material that has a lower conduction band edge than silicon nitride (see, e.g., pp.53/col.1/II.35-43).

8. Regarding claim 6, She shows the gate dielectric having a larger energy barrier between the high-k dielectric and the oxide insulator than silicon dioxide (see, e.g., pp.53/col.1/II.45-48).

9. Regarding claim 7, She shows the gate dielectric has an oxide-Hf oxide-oxide structure (see, e.g., fig. 1).

10. Regarding claims 1, 2, and 7, it is noted that She shows all aspects of the semiconductor device according to the claimed invention (see, e.g., paragraphs 6 and 7 above) and that the method of forming an oxidized metal gate dielectric by the low-temperature oxidation of a metal, is an intermediate step that does not affect the structure of the final device.

In spite of the above, Ahn (see, e.g., par. 0029) uses a low-temperature oxidation step to form an oxidized metal gate dielectric similar to She. Ahn teaches that doing so would result in the oxidized metal gate dielectric having a high growth rate, high dielectric strength, and low interface trap and bulk charge (see, e.g., col.6/II.5-8).

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to form She's gate dielectric by the low temperature oxidation of a metal, as suggested by Ahn, because doing so would result in a gate dielectric having low interface trap and bulk charge.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over She/Ahn in view of Akatsu (US 5717635).

12. Regarding claim 4, She shows most aspects of the instant invention (see, e.g., paragraph 5 above). She, however, fails to show that the transistor is in either a NOR-type flash memory structure or a NAND-type flash memory structure. She, however, teaches that the transistor is a flash-EEPROM device (see, e.g., abstract). At the present time, there are two basic architectures for EEPROM memory cell arrays referred to as NOR-type and NAND-type respectively (see, e.g., Akatsu/col.4/ll.50-57). The NAND-type, however, lends itself to much higher integration densities (see, e.g., Akatsu/col.5/ll.34-40).

It would have been obvious at the time of the invention to one of ordinary skill in the art to have She/Ahn's transistor in a NAND-type memory structure, as suggested by Akatsu, to achieve a high-integration density.

Response to Arguments

13. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

15. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through

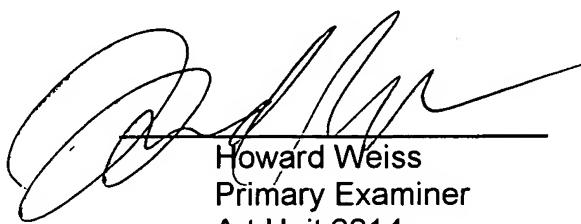
Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

18. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

19. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/314,324-326,410,411	12/7/2005
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	12/7/2005

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December 7, 2005



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